Amendments to the Title

Please change the title to the following: -- Method of Fabricating Integrated Circuitry, and Method of Forming a Conductive Line --.

Amendments to the Specification

At page 1 before the "Technical Field" section, please insert the following:

--RELATED PATENT DATA

This patent resulted from a divisional application of U.S. Patent Application Serial No. 10/418,540, filed April 17, 2003, entitled "Method of Forming a Local Interconnect", naming H. Montgomery Manning as inventor, the disclosure of which is incorporated by reference; which resulted from a continuation application of U.S. Patent Application Serial No. 10/087,147, filed February 28, 2002, entitled "Methods of Fabricating Integrated Circuitry", naming H. Montgomery Manning as inventor, now U.S. Patent No. 6,638,842 B2, the disclosure of which is incorporated by reference; which resulted from a divisional application of application of U.S. Patent Application Serial No. 09/608,333, filed June 29, 2000, entitled "Method of Forming a Local Interconnect", naming H. Montgomery Manning as inventor, now U.S. Patent No. 6,391,726 B1, the disclosure of which is incorporated by reference; which resulted from a divisional application of U.S. Patent Application Serial No. 09/266,456, filed March 11, 1999, entitled "Integrated Circuitry, Methods of Fabricating Integrated Circuitry, Method of

Forming Local Interconnects, and Methods of Forming Conductive Lines", naming H. Montgomery Manning as inventor, now U.S. Patent No. 6,180,494, the disclosure of which is incorporated by reference.--

Please amend the paragraph beginning at line 9 on page 8 as follows:

After etching of layer 34, at least one of the exposed sidewalls is covered with insulating material. Such preferably comprises deposition of an insulating layer 46 over substrate 12; lines 22, 24 and 26; and planarized and etched insulative material 34 to a thickness which less than completely fills at least some of the contact openings (Fig. 6). Such layer preferably comprises a spacer forming layer, with silicon dioxide and silicon nitride being but two examples.

Please amend the paragraph beginning at line 16 on page 11 as follows:

Referring to Fig. 9, local interconnect layer 56 is formed (i.e., by photopatterning and etching) into a local interconnect line 57 which overlies at least portions of illustrated conductive lines ~~24, 26 and 28~~ 22, 24 and 26, and electrically interconnects substrate material locations 42, 43 and 44.